

# Noise-assisted Multibit Storage Device

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## Abstract

In this paper we extend our investigations on noise-assisted storage devices through the experimental study of a loop composed of a single Schmitt trigger and an element that introduces a finite delay. We show that such a system allows the storage of several bits and does so more efficiently for an intermediate range of noise intensities. Finally, we study the probability of erroneous information retrieval as a function of elapsed time and show a way for predicting device performance independently of the number of stored bits.

## 1 Introduction

In the last few years there has been an increased effort in the search of alternative technologies for computer memory devices (see, e.g., [19] and references therein). This effort is motivated by the perceived near-future end of the ability of current technologies to provide support for the exponential increase of memory capacities as predicted by Moore's law. In this context, we have worked on the concept of memories which can benefit from (and, indeed, work only in) the presence of noise which is typically found in electronic circuits. In a similar vein, logic gates that work with the help of noise have been suggested in, e.g., Refs. [17, 16]. Building on the work of Refs. [2, 3], where a ring of identical oscillators was shown to be able to sustain a traveling wave with the aid of noise long after the harmonic drive signal had been switched off, we showed that a ring of two bistable oscillators is capable of storing a single bit of information in the presence of noise [4, 8, 18]. Furthermore, we showed that with the addition of small amounts of white Gaussian noise the system outperformed the deterministic (noiseless) case in terms of the probability of erroneous information retrieval.

In this paper we extend our investigations on noise-assisted storage devices through the experimental study of a loop composed of a single Schmitt trigger

(ST) and an element that introduces a finite delay. We show that such a system allows the storage of several bits and does so more efficiently for an intermediate range of noise intensities. Finally, we study the probability of erroneous information retrieval as a function of elapsed time and describe a way of predicting device performance independently of the number of stored bits.

The proposed memory device can also be considered as a toy model of a long transmission link with in-line nonlinear elements such as saturable absorbers ([11, 5]). An ST approximates the behavior of a saturable-absorber and the delay introduced ad hoc models the natural propagation time of the signal in the transmission line.

Nonlinear delayed loops have been extensively studied (see, e.g., [1, 10, 12, 13, 15, 9, 14]). This type of systems usually present complex nonlinear behavior, including self-sustained oscillations and chaotic operation regimes. Memory devices that make use of regimes that show multistable behavior of delayed feedback loops have been proposed. Ref. [1] presents a memory device that stores bits coded as particular oscillation modes of a delayed feedback loop with an electro-optical modulator. Similarly, it is shown in [12] that binary messages can be stored using controlled unstable periodic orbits of a particular class of delay loop differential equations. However, the memory devices proposed in Refs. [1, 12] are not assisted by noise. Refs. [13] and [9] study the behavior of a delayed loop with a single threshold device and a bi-stable device, respectively, but focusing on the response of the system to a harmonic driving signal.

The remaining of the paper is organized as follows. The working of the proposed device is described in Section 2, while Section 3 presents experimental results. Section 4 closes this work with some final remarks and conclusions.

## 2 Memory device

Fig. 1 shows a scheme of the proposed device. One of its main components is a bistable element, a Schmitt trigger in our case. The output of the ST is delayed and then fed back without any other intended alterations besides the addition of (essentially) white Gaussian noise. It should be noted that the output of the Schmitt trigger is subthreshold, that is, it is incapable of forcing a state change without the assistance of noise. Stored bits are coded as a finite sequence of suprathreshold square pulses. The duration of the sequence is such that it fits entirely in one loop, i.e., it is shorter than or equal to the delay.

In order to retrieve stored bits, the output of the Schmitt trigger must be observed for a time interval equal to the loop delay. In general, a marker is needed to recognize the beginning of a binary message. Since we are not interested in that level of technical detail, in this paper we simply assume that the time elapsed since the bits were stored is perfectly known. Finally,  $n$  stored bits are retrieved by comparing the averages of the output of the Schmitt trigger during  $n$  consecutive intervals to a fixed threshold. In the experiments, the threshold was varied for each set of fixed parameters in order to obtain the lowest probability of error.

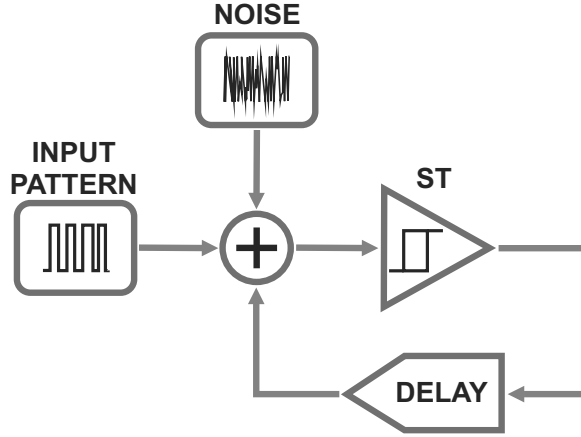


Figure 1: Schematics of the memory device.

### 3 Experimental results

The low and high thresholds of the Schmitt trigger were fixed at  $-1$  V and  $3$  V, respectively, and the low and high output levels were set at  $0$  V and  $2$  V, respectively. The input bit pattern was represented by a sequence of pulses with suprathreshold low and high amplitudes of  $-8$  V and  $10$  V, respectively.

The delay was implemented by means of a in-series pair of 64-bit shift registers clocked with a  $100$  kHz square wave signal. In this way, the output of the Schmitt trigger is effectively sampled at  $100$  kHz and its samples are delayed by  $1.28$  ms. An  $n$ -bit sequence to be stored occupies the full  $1.28$  ms-delay, i.e., each bit occupies  $1280/n$   $\mu$ s. Noise bandwidth was set greater than  $100$  kHz so that it can be regarded as essentially white where most of the input signal power lies.

Fig. 2 shows the probability of error as a function of the noise intensity for different retrieval times when four bits are stored. Each point corresponds to the average of  $1000$  realizations and the stored sequence was  $0110$ . As it is readily observed, there is a range of noise intensities that minimizes the probability of error. Indeed, since the output of the ST is subthreshold, the probability of error is high ( $\sim 1/2$ ) in the absence of noise. The addition of noise helps the subthreshold input signal to drive the Schmitt trigger. Moreover, the probability of a change in the right direction is higher than that in the opposite direction because of the closer proximity to the correct threshold. Therefore, the probability of error initially decreases as the noise intensity increases. However, when the noise intensity is too high with respect to the inter-threshold gap, the probability of error increases because the influence of the driving signal is small with respect to that of noise.

Noise at the input of the Schmitt trigger introduces a random delay with a non-negligible mean value. In fact, such delay may be profitably used to

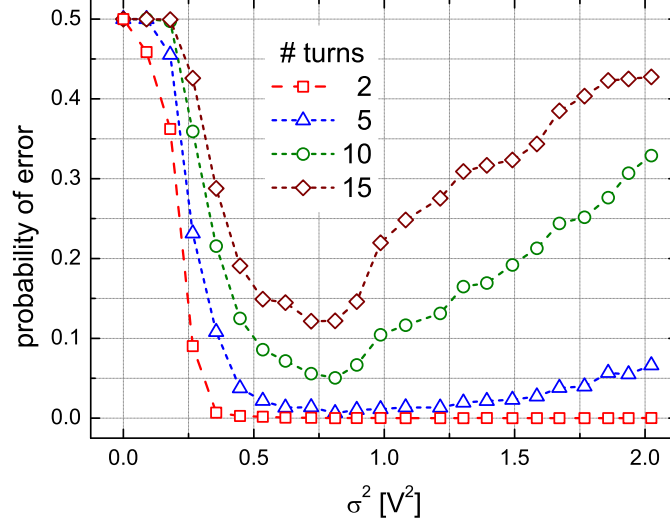


Figure 2: Probability of error vs. noise intensity when four bits are stored. Different curves correspond to varying elapsed times.

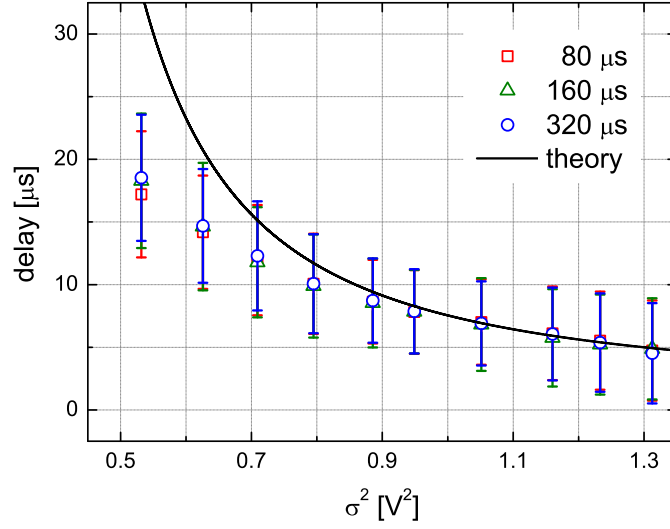


Figure 3: Mean and standard deviation of the random delay vs. noise intensity. Different curves correspond to different bit lengths. Solid curve: theoretical approximation.

build a noise-tuned delay line on the basis of a chain of bistable devices, as it is explained in, e.g., Ref. [7]. This random delay needs to be taken into account in order to stay synchronized with the output of the ST, by factoring in its mean value as part of the total loop delay. Fig. 3 shows the mean value and the dispersion of the ST delay as a function of the noise intensity. The random delay was estimated based on the cross-correlation between the input and the output of a Schmitt trigger, where the input consisted of 128 randomly generated pulses of fixed duration. Each point in Fig. 3 is the result of averaging 1000 realizations. It is interesting to note that the stochastic delay decreases as the noise intensity ( $\sigma^2$ ) increases. It can also be observed that there is a range of noise intensities for which the standard deviation of the delay is not too high as compared to its mean value, i.e., in this range timing jitter of the transmitted signal is tolerable. Finally, it must be noted that the delay measured on the basis of the cross-correlation lacks of true meaning in the regions of low and high noise intensities where the output barely resembles the input signal. Fig. 3 also shows a theoretical approximation to the mean delay obtained by modeling noise as an Ornstein-Uhlenbeck (OU) process, with bandwidth  $f_c$  equal to the measured bandwidth. Since the output of the ST follows input transitions whenever the instantaneous noise amplitude is able to bridge the gap to the closest threshold ( $\Delta V = 1$  V), we approximated the delay by the expected time for the OU process to go from 0 V (its stationary mean) to  $\Delta V$ , that is (see, e.g., Ch. 5 of Ref. [6])

$$\langle \tau_{tr} \rangle \approx \frac{1}{2\sqrt{\pi}f_c} \int_0^{\frac{\Delta V}{\sqrt{\sigma^2/2}}} e^{x^2} [1 + \text{erf}(x)] dx, \quad (1)$$

where  $\sigma^2$  is the measured noise power. Given that there is essentially no delay when there are no transitions in the driving signal, we estimated the actual mean delay as  $\langle \tau \rangle \approx \langle \tau_{tr} \rangle / 2$ .

The experiment was repeated for 8- and 16-bit sequences. Fig. 4 shows the minimum probability of error ( $p_m$ ) in each case as a function of time. As it can be observed, not only the performance for a given number of bits deteriorates with time, but also with an increasing number of stored bits. This can be understood as follows. The stochastic delay must be short enough so that the ST output is able to follow a transition at its input before the start of the following bit. Since the bit duration decreases as the number of stored bits increases, the noise intensity required to get a shorter random delay increases (Eq. 1) with the number of bits (see Fig. 3). In other words, the optimal noise intensity increases with the number of stored bits. However, a higher noise intensity also implies a higher probability of ST transitions in the wrong direction and, hence, a performance degradation.

Although Fig. 4 points to a performance which depends on the number of bits stored, there is a scaling that allows a unified description. Indeed, as Fig. 5 shows, the probability of error exhibits the same behavior when time is normalized to the bit duration.

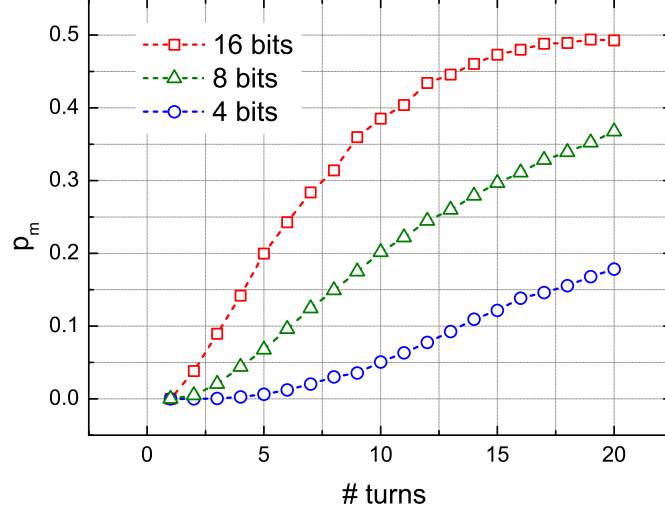


Figure 4: Minimum probability of error vs. elapsed time.

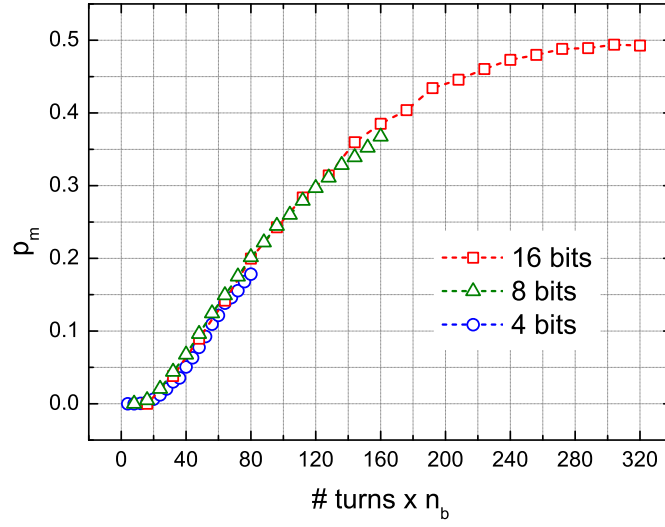


Figure 5: Minimum probability of error vs. elapsed time normalized to the bit duration.  $n_b$ : number of stored bits.

## 4 Conclusions

In summary, we presented a multibit storage device comprised of a bistable element in a loop configuration which works only with the aid of noise. Moreover, there is a range of noise intensities that minimizes the probability of erroneous information retrieval. In order to measure the probability of error, the random input-output delay at the Schmitt trigger had to be taken into account. We experimentally determined this delay and proposed a theoretical model which agrees very well with measurements.

We also studied the behavior of the minimum probability of error as a function of time. We found that performance deteriorates with time and with the number of stored bits. However, we showed that the probability of error is independent of the number of bits when the elapsed time is normalized to the bit duration, a fact of relevance when considering practical implementations of the proposed memory device.

Finally, we believe that this type of storage devices may be of interest as an alternative technology to push forward the validity of Moore's law as current devices have to deal with decreasing noise margins.

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